THAT WHICH IS CLAIMED IS:

1. A method of fabricating a transistor, the method comprising:

forming a nitride-based channel layer on a substrate;

forming a nitride-based semiconductor first cap layer on the nitride-based channel layer;

forming a mask that covers a first portion of the first cap layer and exposes an adjacent second portion of the first cap layer;

forming a nitride-based semiconductor second cap layer on the exposed second portion of the first cap layer using the mask;

forming a recess on the first portion of the first cap layer adjacent the second cap layer;

forming one of an ohmic contact or a gate contact in the recess; and

forming a corresponding gate contact or ohmic contact on the substrate.

2. A method according to Claim 1, wherein forming a corresponding gate contact or ohmic contact comprises forming the corresponding gate contact or ohmic contact on the second cap layer.

3. A method according to Claim 1:

wherein the mask comprises a conductive material;

wherein forming a recess comprises forming a recess exposing the mask; and

wherein forming one of an ohmic contact or a gate contact comprises forming one of an ohmic contact or a gate contact on the mask in the recess.

4. A method according to Claim 1:

wherein the mask comprises an insulating material;

wherein forming a recess comprises forming a recess exposing the mask; and

wherein forming one of an ohmic contact or a gate contact comprises forming a gate contact on the exposed mask.

5. A method according to Claim 1:

wherein forming a recess comprises removing the mask to expose the first portion of the first cap layer and to form a recess adjacent the second cap layer; and

wherein forming one of an ohmic contact or a gate contact comprises forming one of an ohmic contact or a gate contact on the exposed portion of the first cap layer.

6. A method according to Claim 1:

wherein forming a mask comprises forming a mask that covers spaced apart first portions of the first cap layer and that exposes a second portion of the first cap layer therebetween;

wherein forming a recess comprises removing the mask to expose the first portions of the first cap layer and to form first and second recesses adjacent the second cap layer;

wherein forming one of an ohmic contact or a gate contact comprises forming an ohmic contact in the first recess; and

wherein forming a corresponding gate contact or ohmic contact comprises forming a gate contact in the second recess.

7. A method according to Claim 1:

wherein forming a nitride-based channel layer comprises forming a Group III-nitride layer;

wherein forming a nitride-based semiconductor first cap layer comprises forming a Group III-nitride layer; and

wherein forming a nitride-based semiconductor second cap layer comprises growing a Group-III nitride layer.

8. A method according to Claim 7, wherein the channel layer has a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, and wherein the bandgap of the channel layer is less than the bandgap of the first cap layer.

9. A method according to Claim 7, wherein the channel layer comprises GaN, InGaN, and/or AlInGaN.

10. A method according to Claim 7, wherein the channel layer comprises an undoped layer having a thickness of greater than about 20 Å.

11. A method according to Claim 7, wherein the channel layer comprises a superlattice and/or a combination of Group III-nitride layers.

12. A method according to Claim 7:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN);

wherein the first cap layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN; and

wherein the second cap layer comprises aluminum nitride (AlN), AlInN, AlGaN, GaN, InGaN, and/or AlInGaN.

13. A method according to Claim 7, wherein the first cap layer comprises AlN, AlInN, AlGaN, and/or AlInGaN, and has a thickness of 1 nm to about 10 nm.

14. A method according to Claim 7, wherein the first cap layer is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}.

15. A method according to Claim 7, the first cap layer comprises $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

16. A method according to Claim 15, wherein the first cap layer has a thickness of about 3 nm to about 15 nm.

17. A method according to Claim 7, wherein the first cap layer comprises AlGaN with an aluminum concentration of between about 5% and about 100%.

18. A method according to Claim 17, wherein the first cap layer has an aluminum concentration greater than about 10%.

19. A method according to Claim 7, wherein the first cap layer comprises an AlN layer having a thickness of about 0.3 nm to about 4 nm.

20. A method according to Claim 7, wherein the channel layer has a lower bandgap than the first cap layer.

21. A method according to Claim 1, wherein forming a mask comprises patterning a mask layer using one of a lift-off technique or a wet-etch technique.

22. A method according to Claim 1, wherein forming a mask comprises a forming the mask from a silicon oxide (SiOx), a silicon nitride (SiNx) or an AlN-based material.

23. A method according to Claim 1, wherein the second cap layer comprises the same material as the first cap layer.

24. A method according to Claim 23, wherein the first and second cap layers comprise AlGaN, and wherein the first cap layer has a higher concentration of Al than the second cap layer.

25. A method according to Claim 24, wherein a combined thickness of the first and second cap layers is about 25 nm.

26. A method according to Claim 1, wherein the second cap layer has an orientation such that terminating edges of the second cap layer are not orthogonal to preferred crystal crack directions.

27. A method according to Claim 1, wherein the second cap layer has an Al composition below a level at which a substantial second electron channel forms at a regrowth interface between the first cap layer and the second cap layer.

28. A method according to Claim 1, further comprising forming an additional layer on the second cap layer.

29. A method according to Claim 28, wherein the additional layer comprises at least one of a GaN cap layer, an insulating layer, and a compositionally graded transition layer.

30. A method according to Claim 1, wherein the first and second cap layer each comprise multiple layers.

31. A method according to Claim 1, wherein at least one of the first and second cap layers comprises a nitride-based barrier layer.

32. A method according to Claim 1, further comprising implanting an ohmic contact region of the first cap layer with an n-type dopant before forming the contact in the recess.

33. A method according to Claim 32, wherein implanting an ohmic contact region comprises implanting the ohmic contact region before the growth of the second cap layer.

34. A method according to Claim 1, wherein forming a nitride-based channel layer is preceded by forming a buffer layer on the substrate, and wherein forming a nitride-based channel layer comprises forming the nitride-based channel layer on the buffer layer.

35. A method according to Claim 1:

wherein forming a nitride-based channel layer is preceded by forming a buffer layer on a substrate;

wherein forming a nitride-based channel layer comprises forming a Group III-nitride channel layer on the buffer layer;

wherein forming a nitride-based semiconductor first cap layer comprises forming a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein forming a mask comprises forming a mask covering spaced-apart first portions of the first cap layer and exposing a second adjacent portion of the first cap layer between the first portions;

wherein growing a nitride-based semiconductor second cap layer comprises growing a Group III-nitride second cap layer on the exposed second portion of the first cap layer;

wherein the method further comprises forming a third semiconductor layer on the second cap layer;

wherein forming a recess comprises removing the mask to form recesses that expose the first portions of the first cap layer;

wherein forming one of an ohmic contact or a gate contact comprises forming respective ohmic contacts in the recesses; and

wherein forming a corresponding gate contact or ohmic contact comprises forming a gate contact on the third semiconductor layer.

36. A method according to Claim 35:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H silicon carbide (SiC) substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer with an Al concentration of about 25% and a thickness of about 5 nm;

wherein the second cap layer comprises an n-doped AlGaN layer with an Al concentration of about 20% , a dopant concentration of about 2 X 10^{12} cm^{-2}, and a thickness of about 10 nm; and

wherein the third semiconductor layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 10 nm.

37. A method according to Claim 35:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlN layer having a thickness of about 1 nm;

wherein the second cap layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 20 nm.

38. A method according to Claim 1:

wherein forming a nitride-based channel layer is preceded by forming a buffer layer on a substrate;

wherein forming a nitride-based channel layer comprises forming a Group III-nitride channel layer on the buffer layer;

wherein forming a nitride-based semiconductor first cap layer comprises forming a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein forming a mask comprises forming a mask covering a first portion of the first cap layer and exposing second portions of the first cap layer on opposite sides of the first portion;

wherein growing a nitride-based semiconductor second cap layer comprises growing Group III-nitride second cap layers on respective ones of the exposed second portions of the first cap layer;

wherein the method further comprises forming respective third semiconductor layers on the respective second cap layers;

wherein forming a recess comprises removing the mask to expose the first portions of the first cap layer;

wherein forming one of an ohmic contact or a gate contact comprises forming a gate contact on the exposed portion of the first cap layer; and

wherein forming a corresponding gate contact or ohmic contact comprises forming respective ohmic contacts on the third semiconductor layers.

39. A method according to Claim 38:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer having a thickness of about 25 nm and an aluminum concentration of about 25%;

wherein the second cap layers comprises undoped AlGaN layers having a thickness of about 5 nm and an aluminum concentration of about 20%;

wherein the third semiconductor layers comprise doped AlGaN layers having a thickness of about 10 nm and an aluminum concentration of about 20%.

40. A method according to Claim 1, wherein forming a nitride-based semiconductor second cap layer comprises growing the second cap layer on the exposed portion of the first cap layer.

41. A method according to Claim 1, where the channel layer and the first and second cap layers are configured to provide a High Electron Mobility Transistor (HEMT).

42. A method of fabricating a contact for a nitride-based microelectronic device, the method comprising;

forming a nitride-based semiconductor first layer on a substrate;

forming a mask that covers a first portion of the first layer and exposes an adjacent second portion of the first layer;

forming a nitride-based semiconductor second layer on the exposed portion of the first layer using the mask;

forming a recess on the first portion of the first cap layer adjacent the second layer; and

forming a contact in the recess.

43. A method according to Claim 42:

wherein the mask comprises a conductive material;

wherein forming a recess comprises forming a recess exposing the mask; and

wherein forming a contact comprises forming a contact on the mask in the recess.

44. A method according to Claim 1:

wherein forming a recess comprises removing the mask to expose the first portion of the first layer and to form a recess adjacent the second layer; and

wherein forming a contact comprises forming a contact on the exposed portion of the first layer.

45. A method according to Claim 42:

wherein forming a nitride-based semiconductor first layer comprises forming a Group III-nitride layer; and

wherein forming a nitride-based semiconductor second layer comprises growing a Group-III nitride layer.

46. A method according to Claim 42, wherein forming a nitride-based semiconductor second layer comprises growing the second layer on the exposed first portion of the first layer.

47. A transistor, comprising:

a nitride-based channel layer on a substrate;

a nitride-based semiconductor first cap layer on the nitride-based channel layer;

a grown nitride-based semiconductor second cap layer on the first cap layer;

an ohmic contact or a gate contact disposed directly on the first cap layer, adjacent a sidewall of the grown second cap layer; and

a corresponding gate contact or ohmic contact on the substrate.

48. A transistor according to Claim 47, wherein the corresponding gate contact or ohmic contact is on the second cap layer.

49. A transistor according to Claim 46:

wherein the ohmic contact or gate contact disposed directly on the first cap layer comprises an ohmic contact disposed directly on the first cap layer; and

wherein the corresponding gate contact or ohmic contact comprises a gate contact directly on the first cap layer.

50. A transistor according to Claim 47:

wherein the nitride-based channel layer comprises a Group III-nitride layer;

wherein the nitride-based semiconductor first cap layer comprises a Group III-nitride layer; and

wherein the grown nitride-based semiconductor second cap layer comprises a grown Group-III nitride layer.

51. A method according to Claim 50, wherein the channel layer has a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, and wherein the bandgap of the channel layer is less than the bandgap of the first cap layer.

52. A transistor according to Claim 49, wherein the channel layer comprises GaN, InGaN, and/or AlInGaN.

53. A transistor according to Claim 50, wherein the channel layer comprises an undoped layer having a thickness of greater than about 20 Å.

54. A transistor according to Claim 50, wherein the channel layer comprises a superlattice and/or a combination of Group III-nitride layers.

55. A transistor according to Claim 50:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN);

wherein the first cap layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN; and

wherein the second cap layer comprises aluminum nitride (AlN), AlInN, AlGaN, GaN, InGaN, and/or AlInGaN.

56. A transistor according to Claim 50, wherein the first cap layer comprises AlN, AlInN, AlGaN, and/or AlInGaN, and has a thickness of 1 nm to about 10 nm.

57. A transistor according to Claim 50, wherein the first cap layer is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}.

58. A transistor according to Claim 50, the first cap layer comprises $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

59. A transistor according to Claim 58, wherein the first cap layer has a thickness of about 3 nm to about 15 nm.

60. A transistor according to Claim 50, wherein the first cap layer comprises AlGaN with an aluminum concentration of between about 5% and about 100%.

61. A transistor according to Claim 60, wherein the first cap layer has an aluminum concentration greater than about 10%.

62. A transistor according to Claim 50, wherein the first cap layer comprises an AlN layer having a thickness of about 0.3 nm to about 4 nm.

63. A transistor according to Claim 50, wherein the channel layer has a lower bandgap than the first cap layer.

64. A transistor according to Claim 47, wherein the second cap layer comprises the same material as the first cap layer.

65. A transistor according to Claim 64, wherein the first and second cap layers comprise AlGaN, and wherein the first cap layer has a higher concentration of Al than the second cap layer.

66. A transistor according to Claim 65, wherein a combined thickness of the first and second cap layers is about 25 nm.

67. A transistor according to Claim 47, wherein the second cap layer has an orientation such that terminating edges of the second cap layer are not orthogonal to a preferred crystal crack direction.

68. A transistor according to Claim 47, wherein the second cap layer has an Al composition below a level at which a substantial second electron channel forms at a regrowth interface between the first cap layer and the second cap layer.

69. A transistor according to Claim 47, further comprising an additional layer on the second cap layer.

70. A transistor according to Claim 69, wherein the additional layer comprises at least one of a GaN cap layer, an insulating layer, and a compositionally graded transition layer.

71. A transistor according to Claim 47, wherein the first and second cap layers each comprise multiple layers.

72. A transistor according to Claim 47, wherein at least one of the first and second cap layers comprises a nitride-based barrier layer.

73. A transistor according to Claim 47, further comprising a buffer layer on the substrate, and wherein the nitride-based channel layer is disposed on the buffer layer.

74. A transistor according to Claim 47:

wherein the nitride-based channel layer comprises a Group III-nitride channel layer on a buffer layer;

wherein the nitride-based semiconductor first cap layer comprises a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein the grown nitride-based semiconductor second cap layer comprises a grown Group III-nitride second cap layer on the exposed second portion of the first cap layer;

wherein the transistor further comprises a third semiconductor layer on the second cap layer;

wherein an ohmic contact or a gate contact comprises respective ohmic contacts adjacent opposite sidewalls of the second cap layer; and

wherein the corresponding gate contact or ohmic contact comprises a gate contact on the third semiconductor layer.

75. A transistor according to Claim 74:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H silicon carbide (SiC) substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer with an Al concentration of about 25% and a thickness of about 5 nm;

wherein the second cap layer comprises an n-doped AlGaN layer with an Al concentration of about 20% , a dopant concentration of about 2 X 10^{12} cm^{-2}, and a thickness of about 10 nm; and

wherein the third semiconductor layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 10 nm.

76. A transistor according to Claim 74:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlN layer having a thickness of about 1 nm;

wherein the second cap layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 20 nm.

77. A transistor according to Claim 47:

wherein the nitride-based channel layer comprises a Group III-nitride channel layer on a buffer layer;

wherein the nitride-based semiconductor first cap layer a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein the grown nitride-based semiconductor second cap layer comprises grown Group III-nitride second cap layers on respective spaced apart portions of the first cap layer;

wherein the transistor comprises forming respective third semiconductor layers on the respective second cap layers;

wherein an ohmic contact or a gate contact comprises a gate contact on a portion of the first cap layer between the second cap layers; and

wherein a corresponding gate contact or ohmic contact comprises respective ohmic contacts on the third semiconductor layers.

78. A transistor according to Claim 77:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer having a thickness of about 25 nm and an aluminum concentration of about 25%;

wherein the second cap layers comprises undoped AlGaN layers having a thickness of about 5 nm and an aluminum concentration of about 20%;

wherein the third semiconductor layers comprise doped AlGaN layers having a thickness of about 10 nm and an aluminum concentration of about 20%.

79. A transistor according to Claim 47, wherein the channel layer and the first and second cap layers are configured to provide an HEMT.